Q.P. Code: 18CS0514 **R18**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech III Year I Semester Supplementary Examinations June-2024

COMPILER DESIGN

(Computer Science and Engineering)

Time: 3 hours Max. Marks: 60

PART-A

(Answer all the Questions **5 x 2 = 10** Marks)

1	a	List the various error recovery strategies for a lexical analysis.	L1	2M
	b	Define Ambiguous grammar.	L1	2M
	c	What is bottom up parsing?	L1	2M
	d	Define rules for type checking.	L1	2M
	e	Define Dead-code elimination with example.	L1	2M

PART-B

(Answer all Five Units 5 x 10 = 50 Marks)

UNIT-I

2	a	Write short notes Application of compiler technology.	L1	5M
	b	Write short notes Compiler construction Tools.	L2	5M
		OR		
3		How to design the compiler by using the source program position:=intial+rate*60? Explain.	L1	10M

UNIT-II

4	a	Explain parse trees.	L2	5M
	b	Describe about ambiguity.	L1	5M
		OR		
5		Explain Error recovery in predictive parsing with an Example.	L3	10M

UNIT-III

6		Discuss about YACC tool.	L3	10M
		OR		
7		Explain the Translation scheme of SDD.	L2	10M

UNIT-IV

8		Describe about Control Flow Statements.	L4	10M
		OR		
9		Discuss Storage allocation strategies with suitable examples.	L2	10M

UNIT-V

10		Describe about global data flow analysis.	L2	10M
		OR		
11	a	Write short notes on Simple code generator	L3	5M
	b	Explain the Register allocation and assignment.	L3	5M

END